REMARKS

The Specification and claims have been reviewed for typographical and grammatical errors. A few minor errors were discovered, mostly of a typographical nature, such as a missing word. Various amendatory repairs have been requested. It is believed that none of these is controversial in the least, and that none introduces any new matter whatsoever.

The unknown information in the **Reference To Related Application** on page 1 has brought current.

The ABSTRACT has been shortened.

A missing word ("memory") was added ahead of --tester-- in Claim 6, so as to avoid an antecedent basis difficulty.

As an aid in citing locations in a reference, let us adopt the following notational convention: lines 4 through 23 in col. 7 of Gearhardt are referred to as Gearhardt @ 7:4 - 23. When it is clear that Gearhardt is the reference under consideration, we can simply say 7:4 - 23, and if only line 10 is needed, 2:10. Also, Gearhardt @ 7:4 - 8:41 will be appreciated as indicating line 4 of col. 7 through line 41 of col. 8.

Turning now to the action on the merits, Claim 1 was rejected under 35 USC 102(b) as anticipated by Gearhardt (USP 5,701,309). This rejection is respectfully traversed for the reasons set out below.

As a place to begin, let us first identify what Gearhardt teaches that is relevant to Claims 1-9. First, ATE 25 of Fig. 2 in Gearhardt is, in at least conventional respects, a complete tester in its own right. See 7:14 - 16:

> "During testing of DUT 65, the standard ATE digital tester parallel patterns control the parallel DUT pins (not shown as this is standard). ..."

See also step 320 in Fig. 3: "LOAD ATE TESTER WITH TEST PROGRAM FOR DUT"

It is thus clear that the ATE 25 is capable of at least some form of autonomous action that involves stimulating (and perhaps also checking voltages on) the "mission-oriented" ("parallel") pins of

the DUT; i.e., the pins the designer of the DUT intended the consumer of the DUT to employ when applying the DUT as a part in some circuit.

The DUT is also expected to be one that incorporates the IEEE 1149.1 "Boundary Scan" technique. Referring to Figure 2, this involves sending serial vectors whose totality is initially stored on hard disc 29 (mis-labeled 20 in the Figure, but called 29 at 5:1 - 2 and again at 5: 20 - 23). Portions of interest of the totality for these serial vectors are stored as needed in SRAM 80, and individual vectors sent to the DUT via 105, while expected result serial vectors are received back from the DUT via 110. It will be appreciated that these are JTAG (Boundary Scan) type operations involving the five pin serial JTAG mechanism (the details of which he leaves un-described), and is distinct from what goes on for the other ("parallel" or "mission") pins of the DUT.

So, from a logical perspective, we see that there are two environments that interact with the DUT: the parallel test vectors of the ATE and the serial ones of the JTAG stuff. This now raises the issue of just how these two environments interact, especially given what he says about his purpose of overcoming the shortcoming of a small parallel test vector memory ("pattern memory") in the ATE 25 (see 2:40 -51 and also 4:51 - 59). The answer, such as he provides one, appears to involve hard disc 100 and the overall operational scheme set out in the flow chart of Figure 3. So, for example, at 6:8 - 7:46 we learn that "control vectors" are stored on disc 100, and that they influence what Boundary Scan tests are performed. See especially 6:52 - 7: 13 and the right-hand column of the flow chart in Figure 3. So what he describes is some sort of interleaving of "parallel based" ATE testing with "serial based" Boundary Scan testing. At 7: 18 - 7: 37 he describes a mechanism for the ATE 25 to learn of and respond to a JTAG failure to compare in logic 30, using FAIL signal 55. But as to an exact division of labor between the two environments, well, Gearhardt says very little besides the passage at 5: 58 - 67, nor does he ascribe any particular properties to the DUT, other than it being a part that is susceptible to Boundary Scan testing.

Nevertheless, there is one last topic concerning Gearhardt that interests us, and about which he does give definite information. Gearhardt is going to apply a test stimulus and then check to see if a response is as expected. First, there is (or ought to be) the conventional-for-ATE comparison for the ATE supplied parallel test vectors (the stuff he does not show as "normal" for ATE ...), and second, there is the operation of the COMPARE/CONTROL LOGIC 30 and its FAIL signal 55 (5: 39 - 57). That is,

between the two environments, he applies a stimulus to the DUT and then checks the DUT to see if a response is as expected. Let us inquire about what "expected" means, and how Gearhardt does it.

He uses an ATPG tool to generate a test pattern (6:18 - 22). At 2:32 - 39 he defines a "vector" and also "pattern" -- "pattern" becomes "... a large number of vectors taken together to form a serial data set which fully exercises ... " He then goes on to say that the test pattern is separated into control vectors, a serial input pattern (stimulus) and an expected serial output pattern (response). See 6:22 - 27. The control vectors go onto the disc 100 (step 310 of Figure 3), and the serial input and expected serial output patterns are stored on disc 29 for later use in conjunction with SRAM 80 (6:29 - 31). Along the way the "parallel" vector test program for the ATE proper is loaded into the ATE (6:36 - 38). All of this happens **BEFORE** the test program is begun! See 6:52 - 58. THE ATPG TOOL HAS ALREADY PROVIDED THE CORRECT RESULTS THAT THE ACTUAL TEST RESULTS ARE TO BE COMPARED TO!!

We are now in a position to discuss what is recited in Claim 1, and it will become abundantly clear that Claim 1 is **NOT** anticipated by Gearhardt. Claim 1 is directed to a technique that applicants termed "stimulus log RAM." See line 6 of page 14 through line 25 of page 15, and line 17 of page 39 through line 2 of page 41, all as originally filed. Claim 1 recites in step (a) that a same sequence of transmit vectors is applied to both a memory under test and to a work memory. It appears that either Gearhardt's serial input vector or the ATE's parallel vector would correspond to applicants' transmit vector.

Per step (a): A sequence of transmit vectors is a plurality transmit vectors. At this point in time the claim does not specify if the two memories see one sequence applied to both at once, or if there are first and second applications that occur at separate times (that is for Claims 2 and 3). However, the claim does go on to recite that the application of the sequence of transmit vectors does cause the storing of test pattern data into the memories. One instance of what the recited language means is "write write write write ... write. If there any reads or comparisons that are part of that, we don't know about them -- they would be outside the purview of the claim. The memories are being filled with test pattern data. It is not particularly important to worry about what the test pattern data is -- the test engineer would pick his favorite kind of thing, based on his knowledge of how the DUT is supposed to work or what failure mechanisms it is prone to. The sequence of transmit vectors might, for example, fill the memory with some initial numerical values and then read them out and add them in some sequential pattern that walks

the address space, storing the results back in other locations, until all addresses have been visited some minimum number of times. The work memory is presumed to be a good functional part, and the plan is to compare, **after** the entire sequence is applied, what is in the memory under test with what is in the work memory. (The idea is that the odds are astronomical that there could be any failure along the way and still have a correct comparison at the conclusion of the sequence.) BEFORE THE SEQUENCE WAS APPLIED THERE IS **NO** COPY OF THE CORRECT RESULTS (THE TEST PATTERN DATA)!! WE APPLY THE ENTIRE SEQUENCE TO THE WORK MEMORY TO GENERATE IT DURING THE TEST ITSELF. WE DON'T REMEMBER IT FROM YESTERDAY, OR FROM THE PREVIOUS PART, AND MOST PARTICULARLY, WE DON'T GET IT FROM A PREVIOUS (OFF LINE) USE OF AN ATPG AND THEN STORE IT ON A DISC.

Per step (b), **SUBSEQUENT TO STEP (a)**, the test pattern data content of the memory under test is compared with the test pattern data content of the work memory. That indicates if the memory under test is good or not. So, the claim does not cover a repeat-until-done:[apply stimulus / check response] method, but one of repeated stimuli followed by a final check of under-test (aggregate or end-result) test pattern data against an instance of presumed-correct (aggregate or end-result) test pattern data itself created by the repeated stimuli at the time of the testing, and not already on hand ahead of time.

BUT WE HAVE SEEN THAT GEARHARDT'S COMPARISON DATA IS FOR STEP-AT-A-TIME TESTING, IS CREATED AHEAD OF TIME BY THE ATPG AND IS STORED ON A DISC BEFORE THE TESTING EVER STARTS. GEARHARDT SIMPLY DOES NOT SHOW OR SUGGEST THE METHOD OF CLAIM 1.

It follows then that the various rejections to Claims 2-9 under 35 USC 103 are moot, as those claims all depend on Claim 1. They are, in addition, traversed.

Thus, on the basis of the arguments set out above, claims 1-9 are believed to comply with 35 USC 102 and 35 USC 103, and the Examiner is respectfully, but earnestly, urged to withdraw the rejections.

THEREFORE, re-examination is requested, and favorable action is respectfully solicited.

Respectfully submitted,

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